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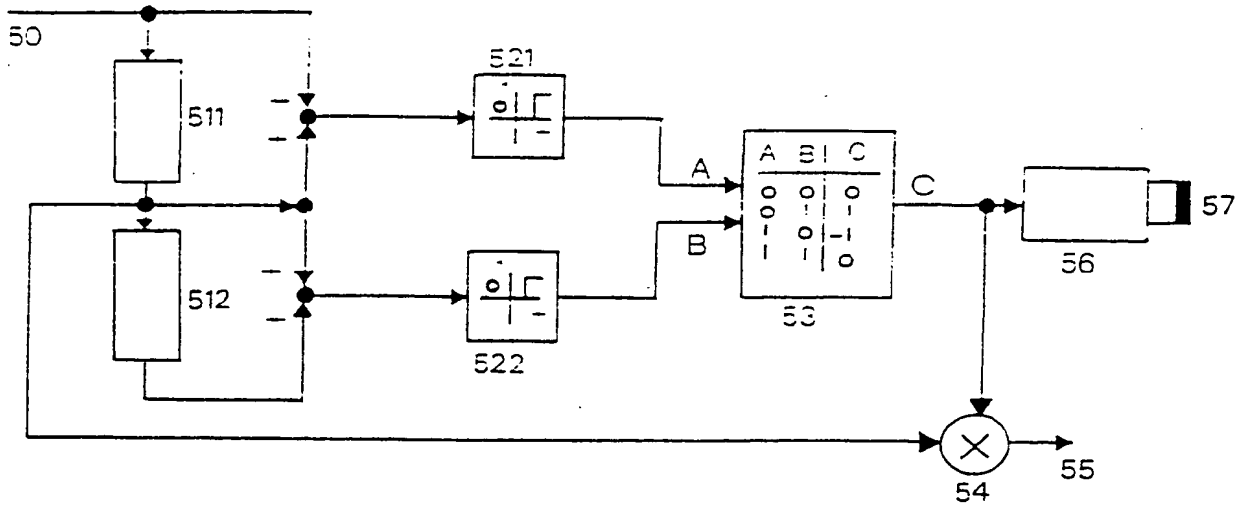
(54) Title: METHOD AND APPARATUS FOR IMPROVING VERTICAL SHARPNESS OF PICTURE TUBES



(57) Abstract

Large format TV tubes must produce a high peak brightness in order to be acceptable to the user. This results in a large beam current in bright areas of the picture and in a subsequent defocussing of the resulting spot on the display and in a loss of the sharpness of vertical and horizontal transitions. The apparent sharpness of a vertical transition is gained by modifying the deflection of the TV receiver such that, at vertical transitions, the line on the bright side of the transition is deflected away from the transition region. Advantageously the amount of vertical scan modulation corresponds to a multi-level control signal and depends on the grey levels of the transition.

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Method and apparatus for improving vertical sharpness of picture tubes

The present invention relates to a method and an apparatus for improving vertical sharpness of images displayed on picture tubes.

Background

Large format TV tubes must produce a high peak brightness in order to be acceptable to the user. This results in a large beam current in bright areas of the picture and in a subsequent defocussing of the resulting spot on the display. Fig. 1 illustrates this effect. The horizontal axis 10 scales the vertical line distances and the vertical axis scales the brightness amplitude. A high brightness spot 12 has a significantly increased diameter compared to a low brightness spot 13. The sharpness of a transition between bright and dark areas is therefore impaired due to an overlapping of the bright spot 22 into a dark region as shown in Fig. 2. The dashed line 25 shows the overall response and the hatched area is a region of impairment 24, whereby line 26 marks the position of the edge in the picture.

Invention

It is an object of the invention to improve the apparent vertical sharpness in transitions between bright and dark picture areas when displayed on TV tubes.

This object will be reached by the features of claim 1. Advantageous additional embodiments are described in the subclaims.

A picture improvement method using a modified vertical deflection is described in the article "Line Flicker Reduction by Adaptive Adjustment of Vertical Deflection in TV Receivers", H.A. Petersen, H.D. Bach, R. Nielsen, IEEE 1990 ICCE Proceedings, FAM 17.3, June 1990. Apparent line flicker is reduced by adaptive adjustment of the vertical deflection. But sharpness impairments caused by varying dot sizes are not eliminated.

An improvement in the apparent sharpness of a vertical transition may be gained by modifying the vertical deflection of a TV receiver such that, at vertical transitions, the line on the bright side of the transition is deflected away from the transition region as shown in Fig. 3. This additional deflection may be provided by means of an additional amplifier and deflection coil on the TV tube. The amount of deflection illustrated in Fig. 3 is of the order of one scan line, but may be less depending upon the characteristics of the display tube. The amount of deflection may also be varied depending upon the characteristics of the video signal, but primarily additional deflections are carried out with a fixed distance either up or down.

Drawings

Preferred embodiments of the invention will now be described with reference to the accompanying drawings, in which:

Fig. 1 is a different-amplitude spot profile;
Fig. 2 shows edge blurring caused by a high brightness spot;
Fig. 3 shows the edge when using the scan modulation according to the invention;
Fig. 4 is an example of a vertical cross section of a TV signal;

Fig. 5 is a block diagram of a control signal generator;
Fig. 6 shows waveforms associated with Fig. 5;
Fig. 7 is an alternative implementation using one full and one 1-bit line delay;
Fig. 8 shows the principle modifications for 4-(or greater-)level comparisons;
Fig. 9 shows a block diagram of an improved control signal generator.

Preferred embodiments

Due to the additional vertical deflection in Fig. 3 the spot 22 in Fig. 2 has now the same location as spot 27 in Fig. 2, so that in Fig. 3 there is only one high brightness dot 32. Superimposing of the both dots results in a higher overall response 35 at this line. The brightness gradient at the edge has increased. A dashed line 36 again marks the edge position.
This method also improves picture quality if the field frequency is higher than 50 or 60 Hz.

An example of a vertical cross-section through an image is shown in Figure 4. Each line and point represents the amplitude of the video signal at one pixel on each line 1 - 14 of the cross-section. It can be seen that in order to improve the display the scan on lines 3, 7, and 9 should be deflected in the direction indicated by the arrows. Transitions also exist at lines 11 and 13, but as this represents a high vertical frequency, no improvement can can be made by modifying the scan, and so the lines should remain undeflected.

A block diagram of a system to implement this processing is shown in Fig. 5.
The incoming video signal 50 is passed through two line delays 511 and 512 to give access to the line following (at

the input of the first line delay 511) and to the line preceding the current line. The line preceding is available at the output of the second line delay 512 and the current line is available at the output of the first line delay 511. Differences are formed between the current line and the following line and between the current line and the previous line. These differences are then passed to a first comparator 521 and to a second comparator 522, respectively, where they are thresholded and converted to binary signals A and B. Then they are combined in a logic circuit 53 to form an output control signal C.
The video signal at the output of the first line delay 511 is fed to an amplifier or multiplier 54, respectively. The gain of this amplifier 54 is controlled by signal C. If C is "0", the gain of amplifier 54 is 1.0, if C is not "0", the gain is about 0.9 in order to reduce the brightness at its output 55.
Signal C is also directed to a deflection circuit 56 which supplies a vertical deflection coil 57.

Figure 6 shows the values of the signals through the processing for the example cross-section of Figure 4, at the point when this signal 61 appears at the output of the first line delay 511. Signal 63 at the input of the first line delay 511 and and signal 62 at the output of the second line delay 512 appear one line later and earlier, respectively. The difference signals 64 and 65 after thresholding appear at points A and B.
It can be seen that point A indicates a signal 66 of lines which should be shifted upwards and point B indicates a signal 67 of lines which should be shifted downwards. Both signals 66 and 67 indicate the same lines in the area of high detail. To provide a control signal output, the signals 66 and 67 are applied to a look-up table in logic circuit 53. The output of this circuit is +1 if only signal A is active or -1 if only signal B is active. If both signals A and B are "0" (no edge detected), or both "1" (a single bright

line), the output is "0" as no improvement can be made by modifying the deflection.

An alternative implementation using only one full resolution video line delay 711 is shown in Figure 7. In this implementation the signals 70, 75, A, B, C and the circuits 711, 721, 722, 73, 74, 76 and the coil 77 correspond to the signals 50, 55, A, B, C, and the circuits 511, 521, 522, 53, 54, 56, and the coil 57 in Figure 5.
An unity gain inverting amplifier 78 is added, but the line delay 712 has only 1-bit resolution. The 1-bit control signal at the output of the second comparator 722, corresponding to signal A in Figure 5, is delayed by one line before being applied to the lookup table within logic circuit 73.

When the control signal C deflects the scanning beam, this results in perceivable increase in brightness on the display for the part of the image for which the original and deflected parts of scan lines overlap. For both implementations, a reduction of the amplitude of the video signal within switched gain amplifier 54, 74 may be made when the control signal C is active. If the reduction in brightness is too great, visible edge busyness results along contours near the threshold. A value of about 0.9 appears to provide a good compromise between edge busyness and a suitably reduced increase in brightness of the overlapping parts of the scan.

At the expense of greater hardware complexity in the line delays and decision circuitry, the control signal C can be made to have an amplitude depending on the video contour. Then the output of the comparators 521, 721, 522, 722 is a multi-level signal, which is applied to the logic circuit 53, 73. An example transfer characteristic of a 4-level comparator is shown in Figure 8a. Obviously, the 1-bit line delay 712 in Figure 7 now requires the number of bits necessary to represent the comparator output. The look-up table in logic circuit 53, 73 is now expanded and is shown in tabu-

lar form in Figure 8b. To illustrate the principle, comparator outputs with 2-bit resolution are shown. Essentially, the control signal C increases in proportion with the comparator's values for the case of a single edge. In the case of high frequency detail (output from both comparators at A and B) the control signal is inhibited in the normal way.

Control signal C can also be obtained by using the information available during a field rate upconversion process.

Fig. 9 depicts a block diagram on basis of the block diagram of Fig. 5. Incoming video signal 90, line delays 911 and 912, comparators 921 and 922, logic circuit 93, amplifier 94, deflection circuit 96 and deflection coil 97 respect the corresponding circuits and signals of Fig. 5.
The output control signal C generated in logic circuit 93 is fed also to a second logic circuit 98 and to staircase circuit 99. Deflection circuit 96 is not controlled by output control signal C but by the according output signal OUT of staircase circuit 99. The inputs of comparators 922 and 921, respectively, are connected to the inputs IN1 and IN2, respectively, of second logic circuit 98. The output of this circuit is either the signal at input IN1 or at input IN2 or at input IN3 (= 0) and is fed with relation to output control signal C to input IN of staircase circuit 99. The output of second line delay 912 is fed to a third comparator 981 and input video signal 90 is fed to a fourth comparator 982. The second input of each of these comparators is connected to a voltage MINGREY. The output signals of these comparators are inputted to an AND circuit 983 which is connected to a switch 984. The output signal of switch 984 is also fed to staircase circuit 99.

The applied additional vertical deflection (of ±1 line) may destroy the equally spaced scanning grid and introduces holes at the darker side of a transition after the postfil-

tering by the beam current. Obviously these holes remain unvisible if at the darker side of the edge the beam current remains nearly zero. But for grey levels the holes coming up may be annoying. This effect becomes even more disturbing if the vertical transition extends not over one but two lines as it is the case after a vertical upconversion by an interpolating filter. With an interpolated value halfway between the value of both sides of the edge corresponds a smaller cross section of the electron beam and therefore less overlapping with the adjacent lines.

Therefore in case of vertical transitions between grey and white levels the deflection amplitude will be reduced. Although the holes cannot be avoided a good compromise between edge enhancement and artefacts can be achieved with a circuit according to Fig. 9. Depending on the actual values of output control signal C, of the signal at input IN and the output signal of switch 984 different staircase functions are generated within staircase circuit 99.

The signal at input IN represents the transition amplitude. When this amplitude increases continuously the signal at output OUT will increase stepwise if $C > 0$ or $C < 0$.

If one or both input signals of the third and the fourth comparators 981 and 982 are less than voltage level MINGREY the output signal of switch 984 will be zero, i.e. graph 'DIV = 0' in staircase circuit 99 is valid. If both comparator input signals are greater than MINGREY the output of AND circuit 983 will go high and switch 984 passes a dividing value DIV > 0 to staircase circuit 99. According to value DIV the slope of the generated staircase function is changed. Six different graphs (one half of each graph, the graphs are symmetrical to axis OUT = 0) corresponding to value DIV are shown in Fig. 9. If DIV ≥ 6, the signal at output OUT is zero regardless of the level at input IN. Preferred values are:

MINGREY = 160 ... 200 within the full range 0 ... 255 (8 bit) of video signal 90

DIV = 2

For improving noise immunity with respect to output control signal C this signal can be a multilevel control signal of at least three bit resolution in conjunction with an horizontal low pass filter. Thereby 'busy edges' are avoided. The line delays, comparators, logic circuits and the staircase circuit are then made matching for such higher resolution. In order to also avoid an additional deflection in uniform picture parts, which can happen due to transients of a usual lowpass filter after the electron beam has passed a horizontal edge, an edge preserving filter, e.g. a median filter, is applied (not depicted).

Claims

1. Method for improving vertical sharpness of pictures displayed with a line structure on a picture tube, characterized in that the beam of said tube is deflected in vertical direction in relation to vertical bright-ness transitions.

2. Method according to claim 1, characterized in that said deflection in vertical direction is composed of a known vertical deflection and an additional vertical deflection.

3. Method according to claim 2, characterized in that said additional vertical deflection is such that within bright areas (22) at vertical brightness transitions the beam is deflected away to the bright side of said transition region.

4. Method according to claim 3, characterized in that said additional vertical deflection is active if said bright area has a height of more than one line.

5. Method according to any of claims 2 to 4, characterized in that the amount of said additional vertical deflection relates to the slope of said transition.

6. Method according to any of claims 2 to 5, characterized in that the amount of said additional vertical deflection relates to the grey levels of said transition.

7. Method according to any of claims 2 to 6, characterized in that the amount of said additional vertical deflection is a staircase function relating to the grey levels of said transition.

8. Apparatus using a method according to any of claims 1 to 7, characterized in that said apparatus comprises two or more line delays (511, 512, 711, 712, 911, 912) which are followed by two or more comparators (521, 522, 721, 722, 921, 922), forming binary output signals (A, B), combining said output signals in one or more logic circuits (53, 73, 93, 98) which forms a control signal (C) consisting of at minimum three levels and using said control signal for generating said additional vertical deflection and for reducing the amplitude of said brightness signal in a multiplier (54, 74, 94).

9. Apparatus according to claim 8, characterized in that one (712) of said two or more line delays (711, 712) is located between one (722) of said comparators (721, 722) and one of said logic circuits (73).

10. Apparatus according to claim 8 or 9, characterized in that said comparators (521, 522, 721, 722, 921, 922) generate said output signals (A, B) with more than two levels and that said logic circuit (53, 63) accordingly generates said control signal (C) with more than three levels.

11. Apparatus according to any of claims 8 to 10, characterized in that said control signal (C) is fed to a staircase circuit (99) wherein said control signal is changed corresponding to the grey levels of said transition.

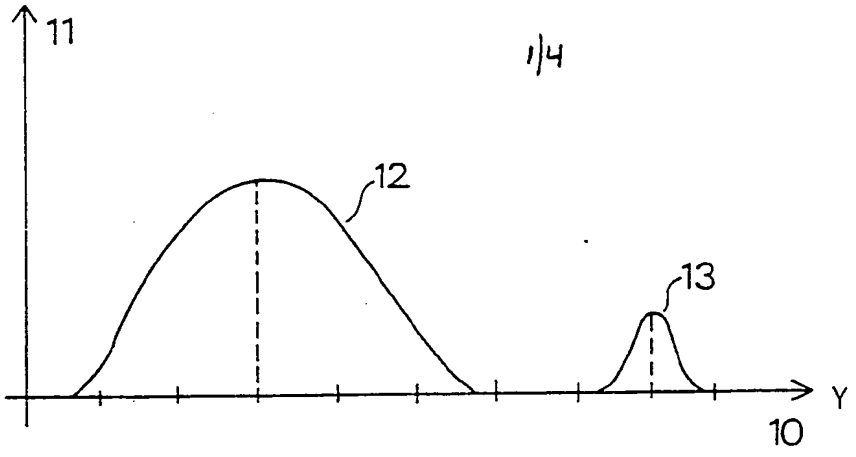


FIG.1

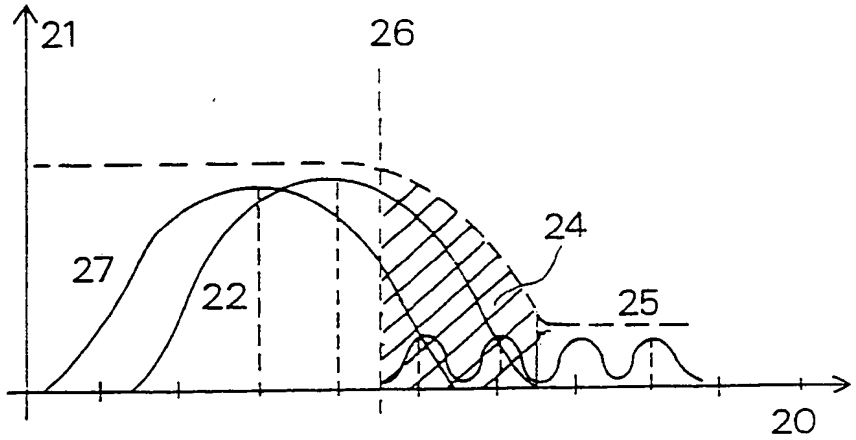


FIG.2

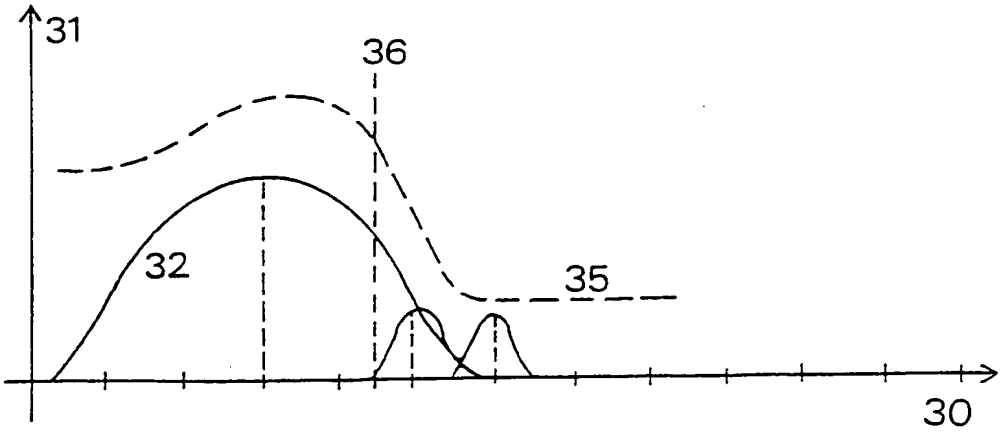


FIG.3

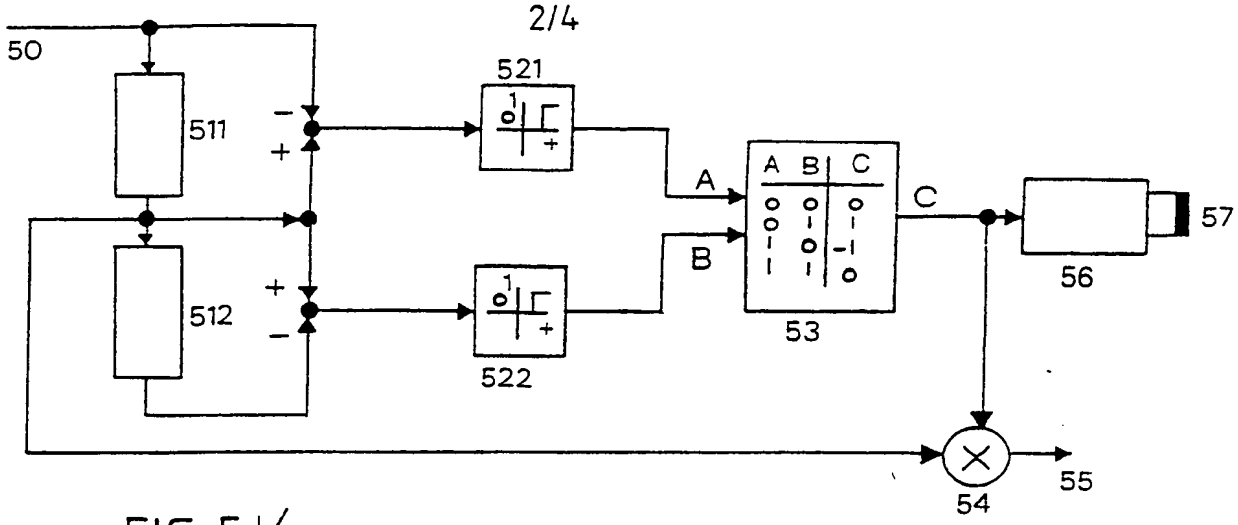


FIG. 5

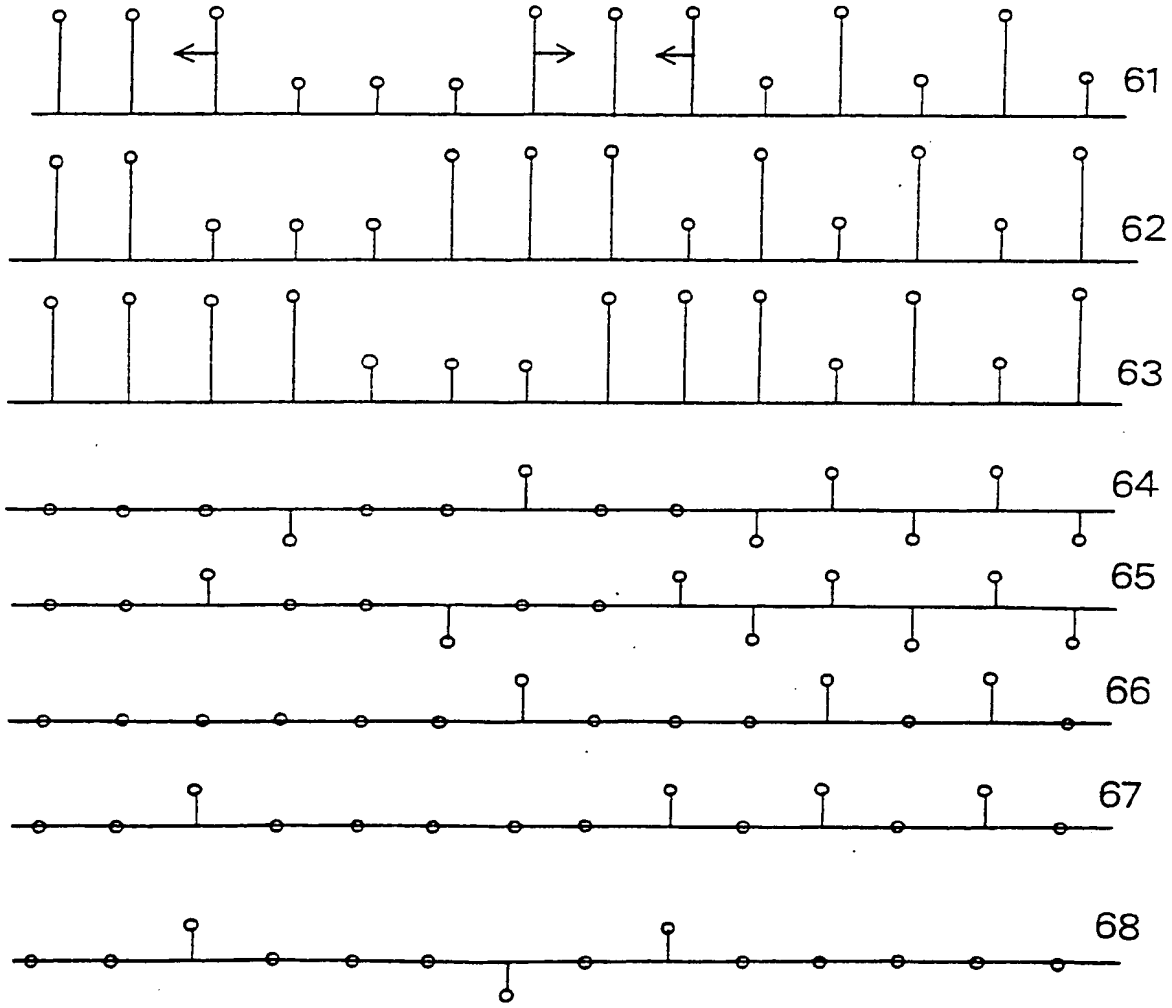


FIG.6

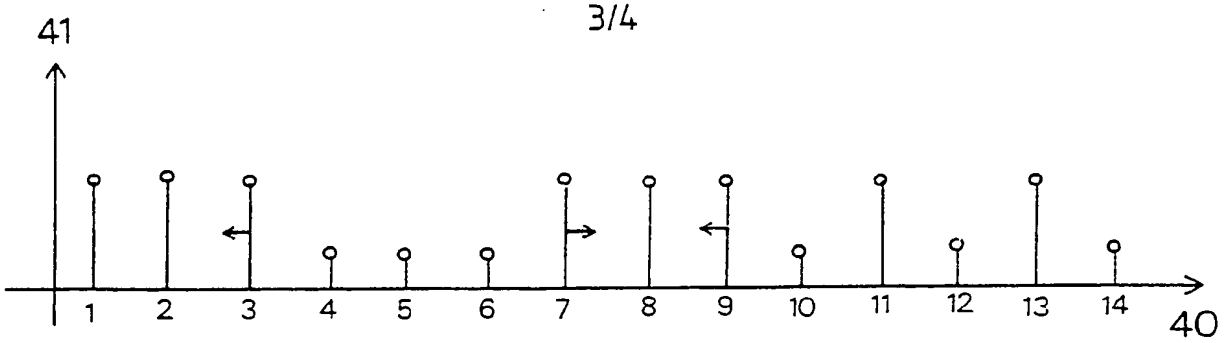


FIG.4

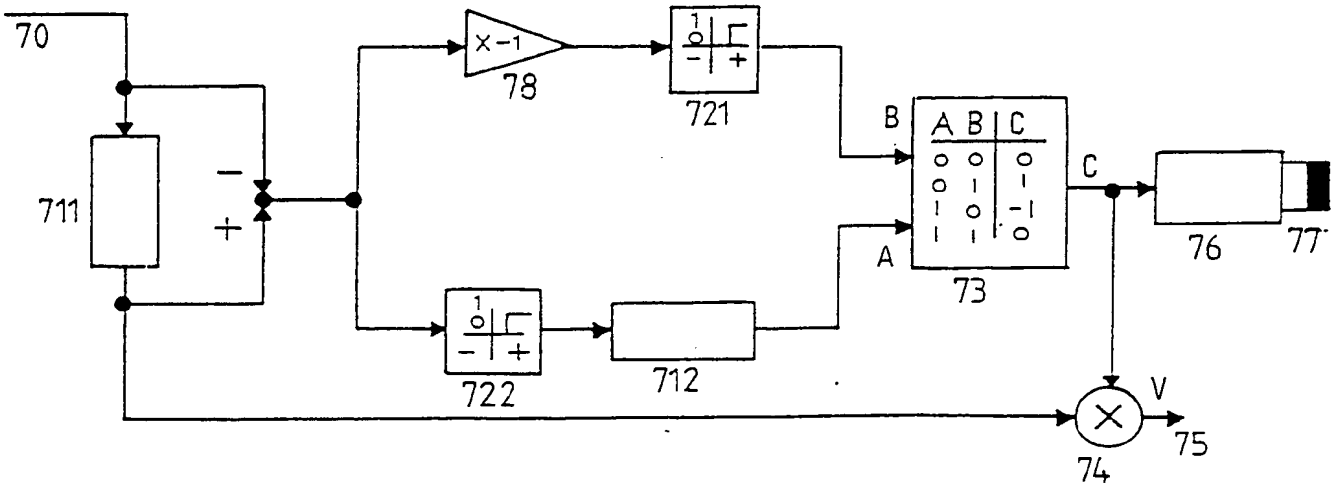
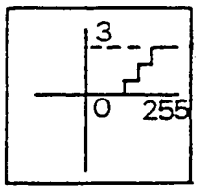


FIG.7



(a)

(b)

B \ A	0	1	2	3
0	0	-0,33	-0,66	-1
1	0,33	0	0	0
2	0,66	0	0	0
3	1	0	0	0

FIG.8

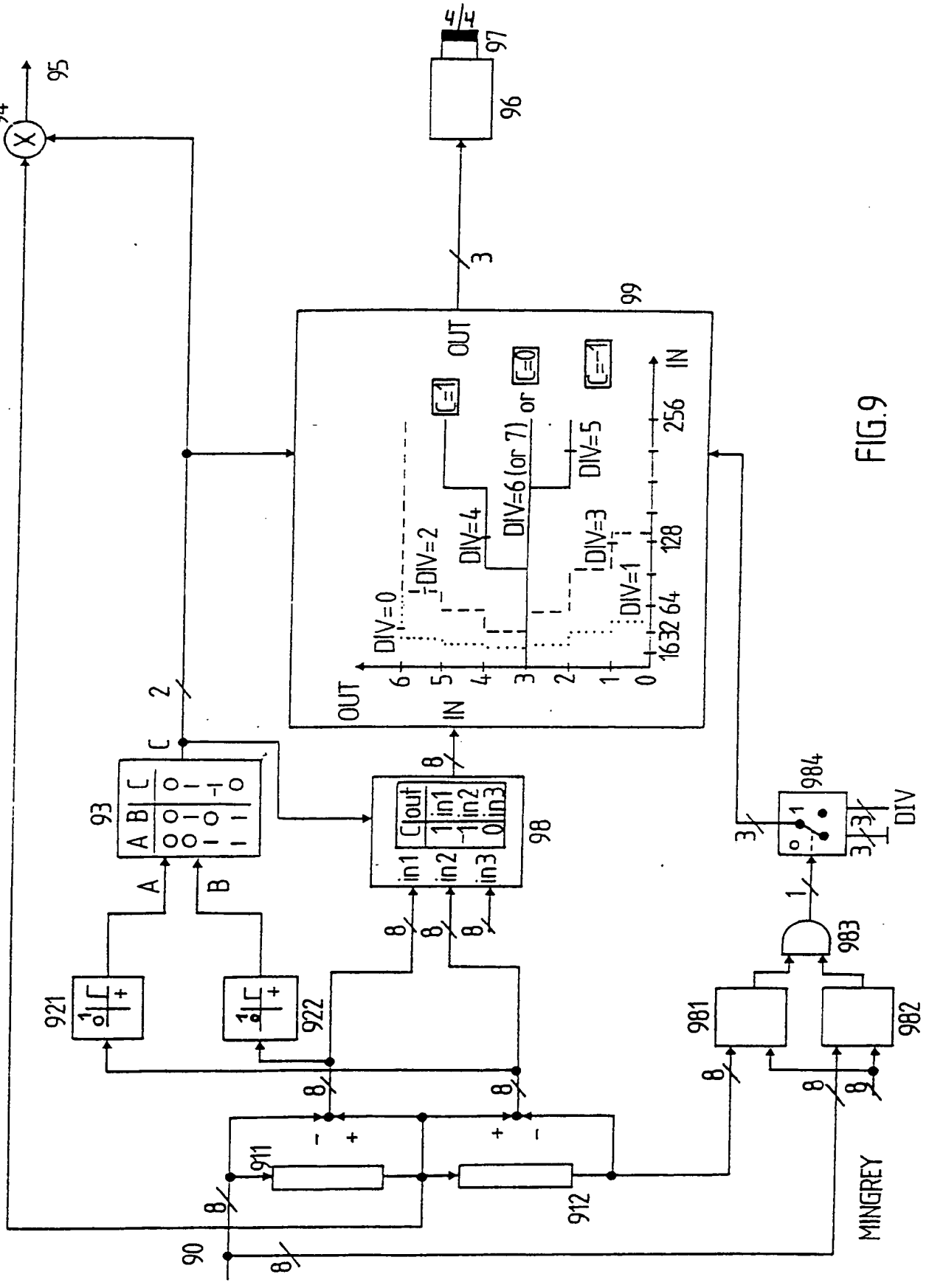

4/4
97
96
95
94
X
3
99
OUT
IN
C=1
C=0
C=-1
DIV=0
DIV=2
DIV=4
DIV=6 (or 7)
DIV=5
DIV=3
DIV=1
1
2
4
8
16
32
64
128
256
6
5
4
3
2
1
0
2
C
93
A B C
0 0 0
0 1 0
1 0 0
1 1 -1
A
B
8
98
Cout
in1
in2
in3
1
-1
0
921
922
911
912
90
MINGREY
981
982
983
984
DIV

FIG.9

INTERNATIONAL SEARCH REPORT

International Application No PCT/EP 91/01702

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H04N3/30

II. FIELDS SEARCHED

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Classification System	Classification Symbols
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Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No.[13]
X A	US,A,4 888 529 (MADSEN ET AL) 19 December 1989 see column 1, line 1 - column 3, line 57 see column 6, line 57 - column 7, line 63; figure 5	1-6 7,8

X A	DE,A,3 038 144 (PHILIPS) 30 April 1981 see page 5, line 17 - line 30 see page 6, line 35 - page 7, line 11; claim 1	1-5 6-8

X A	US,A,3 530 237 (REDINGTON) 22 September 1970 see column 1, line 42 - column 2, line 59	1-3 4-8

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Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
11 DECEMBER 1991	23. 01. 92
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US-A-4888529	19-12-89	EP-A- 0305017	01-03-89
		JP-A- 1157674	20-06-89
DE-A-3038144	30-04-81	NL-A- 8002410	21-04-81
		AU-B- 536488	10-05-84
		AU-A- 6320180	30-04-81
		FR-A,B 2467517	17-04-81
		GB-A,B 2062401	20-05-81
		JP-C- 1271879	11-07-85
		JP-A- 56065572	03-06-81
		JP-B- 59048591	27-11-84
		SE-B- 452538	30-11-87
		SE-A- 8007147	16-04-81
		US-A- 4347532	31-08-82
		CA-A- 1159555	27-12-83
US-A-3530237	22-09-70	None	

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